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EXAMINER	
LEUNG, CHRISTINA Y	

ART UNIT	PAPER NUMBER
2633	

DATE MAILED: 11/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/025,795	BRISSETTE ET AL.	
	Examiner	Art Unit	
	Christina Y. Leung	2633	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,10-18 and 20* is/are rejected.

7)☒ Claim(s) *9 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *13 Sept. 2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 2, 4, 5, 7, 10-13, and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Cornelius (US 6,885,828 B1).

Regarding claim 1, Cornelius disclose a data regenerator for regenerating a data signal (Figure 2), comprising:

a converter (including comparator 16 and clock and data recovery circuit 18) for converting a received data signal into a binary data signal in dependence on conversion parameters (column 5, lines 1-52);

an error corrector (part of error detection and correction circuit 20) for correcting errors in the binary data signal based on error correction code contained in the binary data signal to produce a corrected binary data signal (column 5, lines 53-67; column 6, lines 1-6); and

a performance monitor (part of error detection and correction circuit 20) for comparing the corrected binary data signal with an uncorrected representation of the binary data signal to determine information about the relative number of logic"1"s and logic "0"s that have been corrected by the error corrector and output a feedback signal representative of the information (column 5, lines 57-67; page 6, lines 1-26);

wherein the converter adjusts at least some of the conversion parameters in dependence on the feedback signal (column 5, lines 8-12; column 6, lines 16-19).

Regarding claim 2, Cornelius discloses that the adjusted conversion parameters include a slicing level for the received data signal to distinguish between a logic "1" and a logic "0" (column 5, lines 8-12 and lines 31-43; column 6, lines 16-19).

Regarding claim 4, Cornelius discloses that the received data signal is an optical data signal transmitted over a fiber path and the converter includes an opto/electrical transducer (photodetector 12) for converting the received data signal into an electrical data signal (column 4, lines 58-60).

Regarding claim 5, Cornelius discloses that the converter includes an analog to digital converter for sampling an analog electrical signal output from the opto/electrical transducer in dependence on the slicing level to produce the binary data signal (comparator 16 receives an analog electrical signal input and outputs a binary data signal; column 5, lines 31-43).

Regarding claim 7, Cornelius discloses the adjusted conversion parameters are adjusted with respect to achieving a threshold balance in the ratio of corrected logic "1"s and "0"s (column 8, lines 49-67; column 9, lines 1-27).

Regarding claim 10, Cornelius discloses that the performance monitor includes counting means for counting a number of logic "1"s and a number of logic "0"s that have been corrected by the error corrector for a predetermined duration of the binary data signal, and outputting signals representative of the number of corrected logic "1"s and corrected logic "0"s (column 8, lines 49-67; column 9, lines 1-27).

Regarding claim 11, Cornelius disclose a method for regenerating a binary data signal (Figure 2) comprising:

converting a received data signal into a binary data signal according to conversion parameters (using comparator 16 and clock and data recovery circuit 18; column 5, lines 1-52);

detecting and correcting errors in the binary data signal based on detection and correction code included in the binary data signal to produce a corrected binary data signal (using error detection and correction circuit 20; column 5, lines 53-67; column 6, lines 1-6);

comparing the corrected binary data signal with an uncorrected representation of the binary data signal to determine information about the relative number of logic "1"s and "0"s that have been corrected (column 5, lines 57-67; page 6, lines 1-26); and

adjusting at least one of the conversion parameters in dependence on the determined information (column 5, lines 8-12; column 6, lines 16-19).

Regarding claim 12, Cornelius disclose that the received data signal is an optical data signal, including converting the optical data signal into an analog electrical signal (using photodetector 12; column 4, lines 58-60) and sampling the analog electrical signal in accordance with a sampling phase to determine, relative to a threshold slicing level, if the samples represent logic "1"s or logic "0"s, to produce the binary data signal (column 5, lines 31-43).

Regarding claim 13, Cornelius disclose that the method of claim 12 including adjusting the threshold slicing level in dependence on the determined information (column 5, lines 8-12; column 6, lines 16-19).

Regarding claim 15, Cornelius discloses that the conversion parameters are adjusted with respect achieving a threshold balance in the ratio of corrected logic "1"s and "0"s (column 8, lines 49-67; column 9, lines 1-27).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 8, 17, 18, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over. Cornelius in view of Kono et al. (US 5,455,536 A).

Regarding claim 8, Cornelius discloses a system as discussed above with regard to claim 1, including means for generally determining when a logic "1" has been corrected to a logic "0" and when a logic "0" has been corrected to a logic "1" by the data regenerator. Cornelius further discloses a duty cycle generator responsive to the first and second signals for generating the feedback signal, the feedback signal being indicative of the ratio of corrected logic "1"s to corrected logic "0"s for predetermined durations of the data signal (Figure 4; column 6, lines 61-67; column 6, lines 1-5).

Cornelius does not specifically disclose receiving a corrected binary data signal and an uncorrected binary data signal from the data regenerator and performing a bit-by-bit comparison of the corrected and uncorrected binary data signals.

However, Kono et al. teach a system related to the one disclosed by Cornelius, including counting bit errors and determining when bits in a data stream have been corrected (Figure 3;

column 3, lines 56-67; column 4, lines 1-18). Kono et al. further teach counting bit errors by receiving a corrected binary data signal (from error corrector 20) and an uncorrected binary data signal (from delay element 22) and performing a bit-by-bit comparison of the corrected and uncorrected binary data signals (column 4, lines 1-10).

It would have been obvious to a person ordinary skill in the art to receive a corrected binary data signal and an uncorrected binary data signal and perform a bit-by-bit comparison of the corrected and uncorrected binary data signals as taught by Kono et al. in the system disclosed by Cornelius as a way to implement the counting of individual bit errors already disclosed by Cornelius.

Regarding claim 17, Cornelius disclose a performance monitoring device for monitoring the performance of a data regenerator that corrects a received data signal based on forward error correction information contained in the received data signal (Figure 2), comprising:

means for comparing the corrected binary data signal with an uncorrected representation of the binary data signal to determine when a logic "1" has been corrected to a logic "0" and when a logic "0" has been corrected to a logic "1" by the data regenerator (column 5, lines 57-67; page 6, lines 1-26);

signal generating means (control circuit 22) for generating an output representative of the relative number of corrected logic "1"s and logic "0"s (column 6 lines 16-31).

Although Cornelius discloses generally determining when a logic "1" has been corrected to a logic "0" and when a logic "0" has been corrected to a logic "1" by the data regenerator, Cornelius does not specifically disclose receiving a corrected binary data signal and an

uncorrected binary data signal from the data regenerator and performing a bit-by-bit comparison of the corrected and uncorrected binary data signals.

Cornelius does not specifically disclose receiving a corrected binary data signal and an uncorrected binary data signal from the data regenerator and performing a bit-by-bit comparison of the corrected and uncorrected binary data signals.

However, Kono et al. teach a system related to the one disclosed by Cornelius, including counting bit errors and determining when bits in a data stream have been corrected (Figure 3; column 3, lines 56-67; column 4, lines 1-18). Kono et al. further teach counting bit errors by receiving a corrected binary data signal (from error corrector 20) and an uncorrected binary data signal (from delay element 22) and performing a bit-by-bit comparison of the corrected and uncorrected binary data signals (column 4, lines 1-10).

It would have been obvious to a person ordinary skill in the art to receive a corrected binary data signal and an uncorrected binary data signal and perform a bit-by-bit comparison of the corrected and uncorrected binary data signals as taught by Kono et al. in the system disclosed by Cornelius as a way to implement the counting of individual bit errors already disclosed by Cornelius.

Regarding claim 18, Cornelius discloses that the signal generating means generates a duty-cycle waveform representative of the ratio of corrected logic "1"s and logic "0"s for a data signal of a predetermined length (Figure 4; column 6, lines 61-67; column 7, lines 1-5).

Regarding claim 20, Cornelius discloses that the signal generating means includes means for counting a number of corrected logic "1"s and a number of corrected logic "0"s for a data signal of a predetermined length, and outputting signals representative of the number of

corrected logic "1"s and the number of corrected logic "0"s (column 5, lines 53-67; column 6, lines 1-6).

5. Claims 3, 6, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cornelius in view of Way et al. (US 6,583,903 B1).

Regarding claims 3, 6, and 14, Cornelius discloses a system and method as discussed with regard to claims 2, 5, and 13 respectively above. Cornelius does not specifically disclose adjusting sampling phase of the signal.

However, Way et al. teach a related data regeneration system including adjusting a threshold level based on feedback (including bit detector 1052 and error detector 1072 in Figure 10), as already similarly disclosed by Cornelius. Way et al. further teach adjusting sampling phase (also known as "sampling timing") in addition to the threshold level (column 5, 25-30; column 6, lines 37-43).

Regarding claims 3, 6, and 14, it would have been obvious to a person of ordinary skill in the art to include adjusting the sampling phase as taught by Way et al. in the system disclosed by Cornelius in order to further optimize the reception of the signal and further minimize errors.

6. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cornelius in view of Lahav et al. (US 2003/0120799 A1).

Regarding claim 16, Cornelius disclose that the received data signal includes a plurality of data frames (column 7, lines 55-67; column 8, lines 1-5) but does not specifically disclose optical transport units. However, optical transport networks are well known in the art as communication protocol, as Lahav et al. particularly teach (pages 1 and 2, paragraphs [0005]-[0009]), and it would have been obvious to a person of ordinary skill in the art to format the data

frames already disclosed by Cornelius as optical transport units as taught by Lahav et al. in order to provide data in a format compatible with known Optical Transport Network systems as an engineering design choice of a type of network.

Allowable Subject Matter

7. Claims 9 and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter:

The prior art, including Cornelius, does not specifically disclose or fairly suggest a data regenerator or performance monitoring means including all the limitations and elements recited in claims 9 or 19 (and including all the limitations of the parent claims on which they depend), particularly including rescrambling an unscrambled corrected binary data signal and an unscrambled uncorrected binary data signal, and providing the rescrambled signals to the comparison means for the bit-by-bit comparison.

Response to Arguments

9. Applicants' arguments filed 13 September 2005 have been fully considered but they are not persuasive.

10. Regarding independent claims 1 and 11 in particular, Examiner respectfully notes that the claims recite "a performance monitor for comparing the corrected binary data signal with an uncorrected representation of the binary data signal" and "comparing the corrected binary data signal with an uncorrected representation of the binary data signal" respectively. Examiner respectfully submits that Cornelius discloses that error detection and correction circuit 20 is an

element that performs the recited function of "comparing the corrected binary data signal with an uncorrected representation of the binary data signal." Circuit 20 provides a corrected binary data signal (column 6, lines 1-6) and also provides a signal which "convey[s] the number of corrected '1's and the number of corrected '0's" (see column 5, lines 53-63). Therefore, Examiner respectfully submits that the circuit must inherently compare the corrected binary data signal with "an uncorrected representation of the binary data signal" in order to determine the number of erroneous 1's and 0's.

In response to Applicants' argument that the references fail to show certain features of Applicants' invention, it is noted that the features upon which Applicants rely (i.e., "a performance monitor that *receives both a corrected data signal and an uncorrected data signal* and compares the signals to determine the relative number of logic 1's and logic 0's that have been corrected" [from page 7 of Applicants' response, emphasis added]) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Examiner respectfully submits that claims 1 and 11 do not specifically recite a comparing function/step beyond "comparing" in an abstract or inherent sense, especially since the claims further recite that the corrected binary data signal is only compared with "an uncorrected representation" of the signal. Examiner acknowledges that the corrected binary signal is explicitly recited in the claims (as the output of the error corrector element) but respectfully submits that the "uncorrected representation" is not explicitly recited as an element in the recited structure.

11. Regarding claim 17 and other claims whose rejections rely on a combination of Cornelius in view of Kono et al., in response to Applicants' arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Again, Kono et al. is relied upon to provide a teaching of implementing a way to compare signals to count bit-by-bit errors or differences between the signals, while Cornelius already discloses providing information about a relative number of corrected 1's and 0's. Also, in response to Applicants' argument that the system of Cornelius in view of Kono et al. would provide a count of the total number of errors instead of the relative number of corrected 1's and 0's, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

Conclusion

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christina Y. Leung whose telephone number is 571-272-3023. The examiner can normally be reached on Monday to Friday, 6:30 to 3:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jason Chan can be reached on 571-272-3022. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-2600.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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